What is claimed is:

1. A method for forming a static pass transistor, comprising:

forming a source region and a drain region in a horizontal substrate;

forming a depletion mode channel in the horizontal substrate between the source and the drain regions;

forming a number of vertical gates above different portions of the depletion mode channel;

wherein forming a number of vertical gates includes forming at least one of the vertical gates separated from the depletion mode channel by a first oxide thickness (t1); and

wherein forming a number of vertical gates includes forming at least one of the vertical gates separated from the depletion mode channel region by a second oxide thickness (t2).

2. The method of claim 1, wherein forming a number of vertical gates above different portions of the depletion mode channel includes forming a number of edge defined vertical gates such that each vertical gate has a horizontal width which is sub-lithographic in dimension.

3. The method of claim 1, wherein forming a number of vertical gates above different portions of the depletion mode channel includes forming a number of logic inputs for the static pass transistor.

4. The method of claim 1, wherein forming the static pass transistor includes forming a NAND logic cell.

5. The method of claim 1, wherein forming at least one of the vertical gates separated from the depletion mode channel by a first oxide thickness (t1) includes forming at least one of the vertical gates as an active input for the static pass

transistor such that the at least one of the vertical gates separated from the depletion mode channel by a first oxide thickness (t1) controls conduction in the depletion mode channel.

6. The method of claim 5, wherein forming at least one of the vertical gates separated from the depletion mode channel by a first oxide thickness (t1) includes forming a first oxide thickness of less than 50 Angstroms (Å).

7. The method of claim 1, wherein forming at least one of the vertical gates separated from the depletion mode channel by a second oxide thickness (t1) includes forming at least one of the vertical gates as a passing line such that the at least one of the vertical gates separated from the depletion mode channel by a second oxide thickness (t1) has a minimal or no control over conduction in the depletion mode channel.

8. The method of claim 7, wherein forming at least one of the vertical gates separated from the depletion mode channel by a second oxide thickness (t1) includes forming a second oxide thickness of less than 150 Angstroms (Å).

9. A method for forming a logic gate transistor, comprising:

forming a source region and a drain region in a horizontal substrate;

forming a depletion mode channel between the source and the drain regions;

forming a first vertical gate located above a first portion of the depletion mode channel and separated from the depletion mode channel by a first oxide thickness;

forming a second vertical gate located above a second portion of the depletion mode channel and separated from the depletion mode channel by a second oxide thickness; and

forming a third vertical gate located above a third portion of the depletion mode channel and separated from the depletion mode channel by the second oxide thickness.

10. The method of claim 9, wherein forming the second and the third vertical gates includes forming the second and the third vertical gates as active inputs for the logic gate transistor such that the second and the third vertical gates control conduction in the depletion mode channel.

11. The method of claim 9, wherein forming the first vertical gate includes forming a passing line such that the first vertical gate has a minimal or no control over conduction in the depletion mode channel.

12. The method of claim 9, wherein forming a first vertical gate separated from the depletion mode channel by a first oxide thickness and forming a second and a third vertical gate separated from the depletion mode channel by a second oxide thickness includes forming a first oxide thickness which has a thickness greater than the second oxide thickness.

13. The method of claim 9, wherein forming the first, the second, and the third vertical gates includes forming edge defined polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

14. The method of claim 13, wherein forming the edge defined polysilicon gates includes forming edge defined polysilicon gates to have a sub-lithographic horizontal width.

15. The method of claim 9, wherein forming a first vertical gate separated from the channel region by a first oxide thickness includes forming a first oxide thickness of approximately 33 Angstroms (Å), and wherein forming a second and a third

vertical gate separated from the channel region by a second oxide thickness includes forming a second oxide thickness of approximately 100 Angstroms (Å).

16. A method for operating a static pass gate transistor, comprising:

applying a potential to a number of vertical gates located above different portions of a horizontal depletion mode channel, wherein at least one of the vertical gates is separated from the depletion mode channel by a first oxide thickness, and wherein at least one of the vertical gates is separated from the depletion mode channel by a second oxide thickness; and

sensing a conduction level through the depletion mode channel.

17. The method of claim 16, wherein applying a potential to the number of vertical gates includes applying the potential to a number of active inputs for the static pass gate transistor.

18. The method of claim 17, wherein applying the potential to the number of active inputs controls conduction in the depletion mode channel such that the static pass gate transistor functions as a NAND gate.

19. The method of claim 17, wherein applying the potential to the number of active inputs includes applying a negative potential of approximately -0.6 Volts to at least one of the active inputs such that the active input turns off conduction in the depletion mode channel.

20. The method of claim 16, wherein applying a potential to the number of vertical gates includes applying the potential to a number of passing lines.

21. A method for operating a logic circuit, comprising:

using a number of vertical gates located above a horizontal depletion mode channel between a single source region and a single drain region to provide an

applied potential above the depletion mode channel, wherein at least one of the vertical gates is separated from the depletion mode channel by a first oxide thickness, and wherein at least one of the vertical gates is separated from the depletion mode channel by a second oxide thickness vertical;

using at least one of the number of vertical gates as a passing line such that a potential on the passing line does not effect conduction in the depletion mode channel; and

using at least two of the number of vertical gates as a number of active inputs such that the active inputs control conduction in the depletion mode channel.

22. The method of claim 21, wherein the method further includes independently applying potential values to the number of vertical gates.

23. The method of claim 22, wherein independently applying potential values to the number of vertical gates includes performing a logic function.

24. The method of claim 23, wherein performing a logic function includes performing a NAND logic function.

25. The method of claim 21, wherein using at least two of the number of vertical gates as a number of active inputs such that the active inputs control conduction in the depletion mode channel includes applying a negative potential to the active inputs of approximately -0.6 Volts to turn off conduction in the depletion mode channel region.

26. The method of claim 21, wherein using at least one of the number of vertical gates as a passing line includes using at least one of the number of vertical gates separated from the depletion mode channel by the second oxide thickness as the passing line, wherein the second oxide thickness is greater than the first oxide thickness.

27. The method of claim 21, wherein the method further includes sensing a conduction level through the horizontal depletion mode channel to sense a state of the logic circuit.

28. The method of claim 21, wherein using a number of vertical gates located above a horizontal depletion mode channel between a single source region and a single drain region to provide an applied potential above the depletion mode channel includes using a number of edged defined vertical gates such that the vertical gates have a horizontal width which is sub-lithographic in dimension.

29. The method of claim 28, wherein using a number of edged defined vertical gates such that the vertical gates have a horizontal width which is sub-lithographic in dimension includes using less than one MOSFET for a number of logic inputs.

30. A method of forming a static pass transistor, comprising;

forming a source region and a drain region on a horizontal substrate;

forming a depletion mode channel in the horizontal substrate between the source region and the drain region;

forming a number of vertical gates above different portions of the depletion mode channel;

wherein forming a number of vertical gates includes forming at least one of the vertical gates separated from the depletion mode channel by a first oxide thickness (t1); and

wherein forming a number of vertical gates includes forming at least one of the vertical gates separated from the depletion mode channel by a second oxide thickness (t2).

31. The method of claim 30, wherein forming a number of vertical gates above different portions of the depletion mode channel includes forming a number of edge

defined vertical gates such that each vertical gate has a horizontal width which has sub-lithographic dimensions.

32. The method of claim 30, wherein forming a number of vertical gates above different portions of the depletion mode channel includes forming a number of logic inputs for a static pass transistor.

33. The method of claim 32, wherein forming the static pass transistor includes forming a NAND logic cell.

34. The method of claim 30, wherein forming at least one of the vertical gates separated from the depletion mode channel by a first oxide thickness (t1) includes forming at least one of the vertical gates as an active input for a static pass transistor such that the at least one of the vertical gates separated from the depletion mode channel by the first oxide thickness (t1) controls conduction in the depletion mode channel.

35. The method of claim 34, wherein the first oxide thickness (t1) is less then 50 Angstroms (Å).

36. The method of claim 35, wherein the first oxide thickness (t1) is about 33 Angstroms (Å).

37. The method of claim 30, wherein forming at least one of the vertical gates separated from the depletion mode channel by a second oxide thickness (t2) includes forming at least one of the vertical gates as a passing line such that the at least one of the vertical gates separated from the depletion mode channel by the second oxide thickness (t2) has a minimal or no control over conduction in the depletion mode channel.

38. The method of claim 36, wherein the second oxide thickness (t2) is less then 150 Angstroms (Å).

39. The method of claim 38, wherein the second oxide thickness (t2) is about 100 Angstroms (Å).

40. A method for forming a logic gate transistor, comprising:

forming a source region and a drain region in a horizontal substrate;

forming a depletion mode channel between the source region and the drain regions;

forming a first vertical gate located above a first portion of the depletion mode channel and separated from the depletion mode channel by a first oxide thickness;

forming a second vertical gate located above a second portion of the depletion mode channel and separated from the depletion mode channel by a second oxide thickness; and

forming a third vertical gate located above a third portion of the depletion mode channel and separated from the depletion mode channel by the second oxide thickness.

41. The method of claim 40, wherein the forming the second and third vertical gates includes forming the second and third vertical gates as active inputs for the logic gate transistor such that the second and the third vertical gates control conduction in the depletion mode channel.

42. The method of claim 40, wherein forming the first vertical gate includes forming a passing line such that the first vertical gate has a minimal or no control over conduction in the depletion mode channel.

43. The method of claim 40, wherein the first oxide thickness is greater then the second oxide thickness.

44. The method of claim 40, wherein forming the first, second and the third vertical gates includes forming edge defined polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

45. The method of claim 44, wherein the edge defined polysilicon gates have a sub-lithographic horizontal width.

46. The method of claim 40, wherein the first oxide thickness is about 33 Angstroms (Å), and the second oxide thickness is about 100 Angstroms (Å).

47. A method for operating a static pass transistor, comprising:

applying a potential to a number of vertical gates located above different portions of a horizontal depletion mode channel, wherein at least one of the vertical gates is separated from the depletion mode channel by a first oxide thickness, and wherein at least one of the vertical gates is separated from the depletion mode channel by a second oxide thickness; and

sensing a conduction level through the depletion mode channel.

48. The method of claim 47, wherein applying a potential to a number of vertical gates includes applying a potential to a number of active inputs for the static pass gate transistor.

49. The method of claim 48, wherein applying the potential to the number of active inputs controls conduction in the depletion mode channel such that the static pass gate transistor functions as a NAND gate.

50. The method of claim 48, wherein applying the potential to the number of active inputs includes applying a negative potential of approximately –0.6 Volts to at least one of the active inputs such that the active input turns off conduction in the depletion mode channel.

51. The method of claim 47, wherein applying a potential to the number of vertical gates includes applying the potential to a number of passing lines.

52. A method of operating a logic circuit, comprising:

using a number of vertical gates located above a horizontal depletion mode channel between a single source region and a single drain region to provide an applied potential above the depletion mode channel, wherein at least one of the vertical gates is separated from the depletion mode channel by a first oxide thickness, and wherein at least one of the vertical gates is separated from the depletion mode channel by a second oxide thickness vertical;

using at least one of the number of vertical gates as a passing line such that a potential on the passing line does not effect conduction in the depletion mode channel; and

using at least two of the number of vertical gates as a number of active inputs such that the active inputs control conduction in the depletion mode channel.

53. The method of claim 52, wherein the method further includes independently applying potential values to the number of vertical gates.

54. The method of claim 53, wherein independently applying potential values to the number of vertical gates includes performing a logic function.

55. The method of claim 54, wherein the logic function is a NAND function.

56. The method of claim 52, wherein using at least two of the number of vertical gates as a number of active inputs such that the active inputs control conduction in the depletion mode channel includes applying a negative potential to the active inputs of approximately –0.6 Volts to turn off conduction in the depletion mode channel region.

57. The method of claim 52, wherein using at least one of the number of vertical gates as a passing line includes using at least one of the number of vertical gates separated from the depletion mode channel by the second oxide thickness as the passing line, wherein the second oxide thickness is greater then the first oxide thickness.

58. The method of claim 52, wherein the method further includes sensing a conduction level through the horizontal depletion mode channel to sense a state of the logic circuit.

59. The method of claim 52, wherein using a number of vertical gates located above a horizontal depletion mode channel between a single source region and a single drain region to provide an applied potential above the depletion mode channel includes using a number of edge defined vertical gates such that the vertical gates have a horizontal width which has sub-lithographic dimensions.

60. The method of claim 59, wherein using a number of edge defined vertical gates such that the vertical gates have a horizontal width which has sub-lithographic dimensions includes using less then one MOSFET for a number of logic inputs.